PQ 60 Standard Document

Version 1.1

Release Date 03/03/2015

Revision History

Version	Date	Section	Changes	Author
0.2				
0.3				
1	16/08/2014	All	New Release based on updated standard	Group
1.001	23/11/2015	All	Changes after review	Group
1.002	12/01/2015	Authors	Update Authors List	Group
		Figure 3.1	Inserted Updated Figure	Group
		Section 6	Link update	Group
		Section 7	Link update	Group
		All	General Text Updates	Group
1.1	03/03/2015	Section 4	Section 4.1 Created	Group
			Section 4.2 Added	Group
			Renamed Section 4	Group
		All	Page Numbers Added	Group

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1. OVERVIEW

This document provides a description of the PocketQube60 (PQ60) standard and the companion standard PQ60 Compatible. This standard covers the internal aspects of a PocketQube design.

The details provided in this document cover the mechanical and electrical interfaces required to design and manufacture a standard PQ60 board. The PQ60 standard was created to provide a starting point for PQ missions and developments. The pin out provided enables the user to access desired basic signals (power and communication).

This standard has been created to help stimulate growth and progression within the PocketQube community. With a standard mechanical and electrical interface for PocketQubes, end users can concentrate on the elements of the PocketQube that interest them the most. The standard will lower barriers of entry for PocketQube programs and will further stimulate growth within the area.

This document continues with an overview of the standard. A description of the mechanical interfaces (board dimensions, mounting points and connection location) is provided followed by a description of the electrical interfaces (connector pin-out and signal descriptions). From this an overview of PQ60 Compatible is provided. The logos for the each of the standards are provided.

This document does not cover PocketQube design nor provide any guidance on any aspects of the design process.

2. STANDARD OVERVIEW

The standard provides for a stack of systems to be connected together to form a PQ. Each system is required to fit within the constraints of a typical PQ structure.

The electrical connections between each board are provided via two stack connectors, one on the bottom of the board, the second on the top. Each signal carried by the connector is required to be passed through the board from the bottom connector to the top connector. This scheme means that every signal is present on every board. If the board requires a particular signal, then this signal is to tapped from the connector.

The signals on the connector were selected to provide the basic requirements for any board: power and communications. The standard allows for:

- 2 protected power buses (3.3V and BatteryV) @ 0.8A each (derated)
- 6 switched power lines (3 x 3.3V and 3 x BatteryV) @ 0.4A each (derated)
- 2 dedicated data buses (I^2C and SPI)
- 12 GPIO lines
- 1 $\overline{SS}$ or GPIO line
- Reset Line

3. MECHNICAL INTERFACES

This section provides the maximum board dimensions, mounting points and the connector locations. The connector used is also documented.

3.1 Board dimensions, mounting points and connector location

Figure 3.1 provides a technical drawing providing information on the maximum board dimensions, mounting points and connector locations. Please note that the board thickness is not provided. The board thickness is dependant on the design of the board. It should be noted that the thickness of the board will have an impact on the overall height of the board.
The dimensions of the board are stated as maximum as boards may require cut-outs.

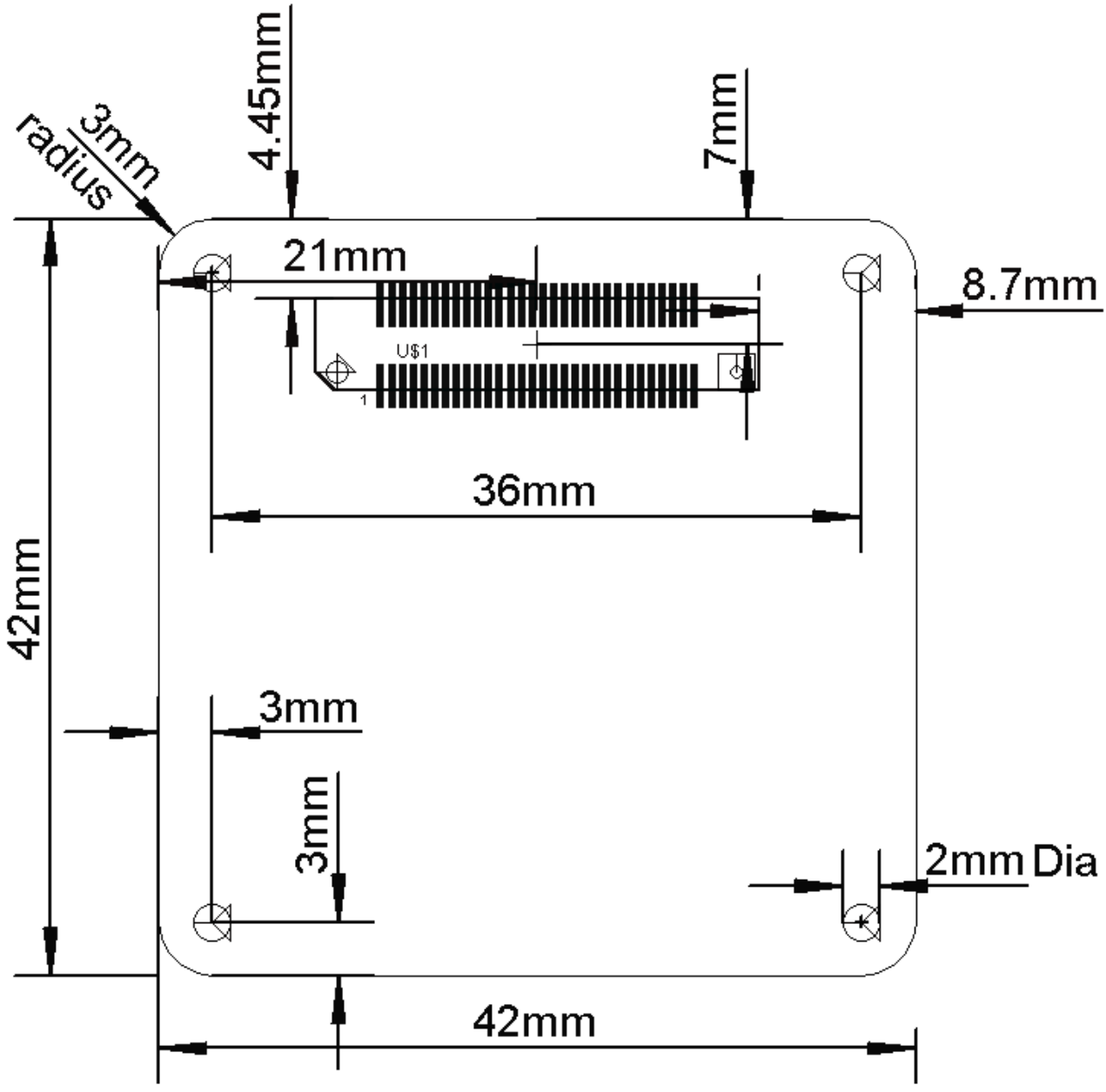

Figure 3.1: Technical drawing of the board

The connector on the top of the board is the *HEADER* version of the standard connector with the connector on the bottom of the board the *RECEPTACLE* version of the standard connector. This was done to allow the topside of the board to determine the height of the full design.

3.2 Connector Information

This section provides information regarding the connector series used. The connector series used is the Hirose FX8C. Details of the series are provided in Table 3.1. The range of heights available using this range are provided in Table 3.2.

Table 3.1: Connector Details	
Series Name	Hirose FX8C
Part Number (excluding height) Header Part Number (excluding height) Receptacle	FX8C-60P-SV FX8C-60S-SV
Pitch	0.6mm
Stacking Height (Connector)	5 – 16 mm
Current Rating (Per Pin)	0.4A (0.2A Derated)
Operating Temperature Range	-55°C to +85°C
Insulator Materials	PBS
Contact Material	Phosphor Bronze

Table 3.2: Connector Heights[1]		
Header	**Receptacle**	
	FX8C-60S-SV	FX8C-60S-SV5
FX8C-60P-SV	5mm	10mm
FX8C-60P-SV1	6mm	11mm
FX8C-60P-SV2	7mm	12mm
FX8C-60P-SV4	9mm	14mm
FX8C-60P-SV6	10mm	16mm

[1] Note that the height is measured between the surface of each board.

4. Pin-out And Electrical Details

The following section describes the pin-out, pin descriptions and electrical details related to the PQ60 standard.

4.1 Pin-out with Pin Descriptions

This section provides the pin-out and electrical details of the connector used. Each signal on the connector is discussed. The relevant information can be found in Figure 4.1 and Table 4.1.

+3.3_Sw1	P1	P60	3V3 bus
+3.3_Sw1	P2	P59	3V3 bus
RTN_SW1_3V3	P3	P58	3V3 bus
RTN_SW1_3V3	P4	P57	3V3 bus
+3.3_Sw2	P5	P56	RTN_3V3
+3.3_Sw2	P6	P55	RTN_3V3
RTN_SW2_3V3	P7	P54	RTN_3V3
RTN_SW2_3V3	P8	P53	RTN_3V3
+3.3_Sw3	P9	P52	BatV bus
+3.3_Sw3	P10	P51	BatV bus
RTN_SW3_3V3	P11	P50	BatV bus
RTN_SW3_3V3	P12	P49	BatV bus
BatV_SW1	P13	P48	RTN_BatV
BatV_SW1	P14	P47	RTN_BatV
RTN_SW1_BatV	P15	P46	RTN_BatV
RTN_SW1_BatV	P16	P45	RTN_BatV
BatV_SW2	P17	P44	GPIO12
BatV_SW2	P18	P43	GPIO11
RTN_SW2_BatV	P19	P42	GPIO10
RTN_SW2_BatV	P20	P41	GPIO9
BatV_SW3	P21	P40	GPIO8
BatV_SW3	P22	P39	GPIO7
RTN_SW3_BatV	P23	P38	GPIO6
RTN_SW3_BatV	P24	P37	GPIO5
GPIO0	P25	P36	GPIO4
GPIO1	P26	P35	GPIO3
/RST	P27	P34	/SS/GPIO2
GND	P28	P33	SCK
SCL	P29	P32	MISO
SDA	P30	P31	MOSI

Figure 4.1: Pin-out for the connector

Table 4.1: Detailed information on the pins			
Pin Number	**Name**	**Function**	**Current, A**
1 + 2	+3.3_Sw1	Switch 1 Output	0.4 (combined)
3 + 4	RTN_SW1_3V3	Switch 1 Return	0.4 (combined)
5 + 6	+3.3_Sw2	Switch 2 Output	0.4 (combined)
7 + 8	RTN_SW2_3V3	Switch 2 Return	0.4 (combined)
9 + 10	+3.3_Sw3	Switch 3 Output	0.4 (combined)
11 + 12	RTN_SW3_3V3	Switch 3 Return	0.4 (combined)
13 + 14	BatV_Sw1	BatV Switch 1 Output	0.4 (combined)
15 + 16	RTN_SW1_BatV	BatV Switch 1 Return	0.4 (combined)
17 + 18	BatV_Sw2	BatV Switch 2 Output	0.4 (combined)
19 + 20	RTN_SW2_BatV	BatV Switch 2 Return	0.4 (combined)
21 + 22	BatV_Sw3	BatV Switch 3 Output	0.4 (combined)
23 + 24	RTN_SW3_BatV	BatV Switch 3 Return	0.4 (combined)
25	GPIO0	General I/O	0.2
26	GPIO1	General I/O	0.2
27	$\overline{\text{RST}}$	Master Reset Line	0.2
28	GND	System Ground	0.2
29	SCL	I^2C Clock Line	0.2
30	SDA	I^2C Data Line	0.2
31	MOSI	SPI MOSI	0.2
32	MISO	SPI MISO	0.2
33	SCK	SPI Clock	0.2
34	$\overline{\text{SS}}$ / GPIO2	Slave Select / General I/O	0.2
35	GPIO3	General I/O	0.2
36	GPIO4	General I/O	0.2
37	GPIO5	General I/O	0.2
38	GPIO6	General I/O	0.2
39	GPIO7	General I/O	0.2
40	GPIO8	General I/O	0.2
41	GPIO9	General I/O	0.2
42	GPIO10	General I/O	0.2
43	GPIO11	General I/O	0.2
44	GPIO12	General I/O	0.2
45 - 48	RTN_BatV	Battery Bus Return	0.8 (combined)
49 - 52	BatV bus	Battery Bus	0.8 (combined)
53 - 56	RTN_3V3	3V3 Bus Return	0.8 (combined)
57 - 60	3V3 bus	3V3 Bus	0.8 (combined)

+3.3V_Sw1-3 / RTN_SW1-3_3V3
These lines are for 3.3V switched power lines. These power lines are designed to be connected to low current systems that are required, or desired, to be switched on and off by the user. It is envisioned that these lines will originate from either a power system or a power distribution board.

BatV_Sw1-3 / RTN_SW1-3_BatV
These lines are for battery voltage switched power lines. These power lines are designed to be connected to low current systems that are required, or desired, to be switched on and off by the user. It is envisioned that these lines will originate from either a power system or a power distribution board.

GPIO 0,1,3-12
These lines are provided to the user for general use. Some examples would be: discrete line control, additional communication lines, analogue lines or any other signal relevant to the system under design.

$\overline{\text{RST}}$ / GND
A dedicated line present on every board on the stack, the RST line, with an associated GND signal, can be used as a master reset line for all systems connected to the stack.

SCL / SDA
An I^2C data bus is provided on these lines.

MOSI, MISO, SCK
These lines provide a SPI bus.

$\overline{\text{SS}}$ / GPIO2
This pin provides either a dedicated $\overline{\text{SS}}$ line for the SPI bus or an additional GPIO line.

BatV Bus / RTN_BatV
A battery bus and return line. This is to be a protected bus, designed to power systems within the PQ. This line will be provided by a power system or power distribution board.

NOTE: *This line should not be used as an unprotected battery bus for the main power source of the PQ.*

3V3 Bus / RTN_3V3
A 3V3 bus and return line. This bus should be a protected bus, designed to power systems within the PQ. This line will be provided by a power system or power distribution board.

4.2 Mounting Holes
The PQ60 standard calls for four mounting holes for each board. Each of these holes should be plated and be connected to *chassis ground* via the mechanical fixings used between each board. This is not ground as described in the Table 4.1 but the chassis ground of the satellite. The user should only connect to the mounting points if there is a requirement for the chassis ground to be used on the board.

The reason for this requirement is to ensure that all boards used in the stack have a common signal through these points. The approach used should protect the user from ground loops and interfacing issues between different boards.

5. PQ60 COMPATIBLE

Not all satellite missions can be based on the same standard and as designs progress new ideas emerge. When this occurs a standard can become a hindrance. To accommodate this the PQ60 Compatible standard can be used.

The PQ60 Compatible standard is to be used for systems that meet the connector and mounting points constraints and have compatible pin-outs. The pin-out does not have to match exactly. For example the connector on the top of the board may match the standard as set down in this document but the bottom connector has been altered to allow connection to a dedicated payload or system. A second example would be reallocation of the switched lines. The PQ may not require three 3.3V switches but needs four BatV switches. One of the 3.3V lines could be re-purposed to be a BatV line. This board would no longer follow the standard as set down but would still be compatible with the standard.

As a baseline a board would be PQ60 Compatible if:

- the power, communication lines and reset line were still in the same location but the GPIO lines were re-purposed
- the voltages of the switches are different
- either the bottom or top connector on the board is compatible

It would be the responsibility of the designer of the board to provide the relevant information to the end user.

6. LOGO'S

There are currently two logos associated with the PQ60 standard. Logo 1 is presented as Figure 6.1 and logo 2 as Figure 6.2. Both logos have been designed to assist users when selecting or researching systems.

Logo 1 is designed to be on documentation for any device or system that is directly compatible with the standard as set out in this document.

Logo 2 is designed for documentation that represents devices or systems that take into consideration the standard and have been tested to be compatible with the standard with either small changes required by the user or certain requirements that need to be met.

It is not a requirement for these logos to be used, but if your device or system meets the standard or is compatible, why not let people know.

Logos are available for download at www.pq60.info

Figure 6.1: PQ60 Standard Logo

Figure 6.2: PQ60 Compatible Logo

7. Updating The Standard

As the standard is used and the PQ community evolves there may be a requirement for the standard to change. To allow this to happen a review of change requests will be done when the request is made. If the PQ60 working group accept the change, this change will be incorporated into the standard within 1 month of the PQ annual conference and the document released. The reason for this is so that there is a known time-line for changes to be made and all changes can be carried out at the one time. With the changes implemented after the PQ conference, discussions at the conference can have an impact on the changes made.

To request or submit a change, please email: *contact@pq60.info*